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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,208	11/19/2001	Kazuyuki Ohhashi	P21699	8111

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GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191

EXAMINER	
AGHDAM, FRESHTEH N	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
12/31/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
pto@gbpatent.com

Office Action Summary	Application No.	Applicant(s)	
	09/988,208	OHHASHI, KAZUYUKI	
	Examiner	Art Unit	
	Freshteh N. Aghdam	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/2007 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 25-35 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato, further in view of the instant application's disclosed prior art.

As to claim 25, Sato teaches a phase offset calculator (Fig. 1, means 102, 201; Fig. 2, means 201, 302, and 303) comprising a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components ; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato does not expressly teach that sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. The instant application's disclosed prior art teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components before being inputted to the phase-offsetter (e.g. SRI and SRQ; Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver.

As to claim 26, Sato discloses a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about when sign of the signed

binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. The instant application's disclosed prior art teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components before being inputted to the phase-offsetter (e.g. SRI and SRQ; Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver. Additionally, Omori discloses a modulator that uses a sign inversion circuit to invert the sign of the input signed binary data and adjusts the amplitude of the sign inverted signal (Fig. 3, means 31 and 36; Col. 2, Lines 29-64). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Omori with Sato and the instant application's disclosed prior art in order to obtain a desired transmission signal by compensating for the amplitude variations of the signal utilizing an amplitude adjuster (Col. 1, Lines 32-36; Col. 2, Lines 56-64).

As to claim 27, Sato further discloses that a fixed phase offset circuitry provides a predetermined amount of a fixed phase offset (Fig. 1, means 108), wherein said fixed phase offset circuitry controls a total phase offset amount with the phase offset implemented by the sign inverter to become a desired offset amount (Col. 4, Lines 44-67, Table I; Col. 5, Lines 37-60, Table II, means 202).

As to claim 28, Sato teaches a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment; and a transmission controller that provides control information to the signal point mapper based on a message included in a reception signal from a receiver that receives communication signals from the CDMA transmission apparatus. The instant application's disclosed prior art teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components before being inputted to the phase-offsetter (e.g. SRI and SRQ; Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal and clearly distinguish between interference signals from other mobile stations and the original reception signal (Pg. 2, Lines 1-5).

As to claim 29, Sato further discloses that a fixed phase offset circuitry that provides a predetermined amount of a fixed phase offset (Col. 4, Lines 44-67, Table I; Col. 5, Lines 37-60, Table II, means 202).

As to claims 30-31, the instant application's disclosed prior art further discloses that the phase and amplitude can be controlled for every transmit channel (Pg. 1, Lines 16-28; Pg. 2, Lines 12-20).

As to claim 32, Sato teaches a phase offset calculator (Fig. 1, means 102, 201; Fig. 2, means 201, 302, and 303) comprising a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation intermediate components; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about when sign of the signed binary data is inverted prior to the amplitude of the signal is adjusted and the phase offsetting is performed after the amplitude adjustment. The instant application's disclosed prior art teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components before being inputted to the phase-offsetter (e.g. SRI and SRQ; Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver.

As to claim 33, Sato teaches a signal mapper for mapping a QPSK modulation signal comprising: a sign inversion circuit that performs a sign inversion of input signed binary data to a phase offset Θ of multiple 90° to output the phase offset calculation

intermediate components; a phase offset circuit that performs a phase offset calculation smaller than 90° with the signal output from the phase shifter 201 (Fig. 1,means 202; Col. 4, Lines 44-67; Col. 5, Lines 1-53). Sato is silent about controlling the phase offsetting based on a signal from a remote source. The instant application's disclosed prior art teaches a transmission controller that provides control information from a remote source to the phase offsetting circuit (Pg. 1, Lines 16-28; Pg. 2, Lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art to control the operation of the phase offsetting circuitry based on a control signal received from a remote source as taught by the instant application's disclosed prior art in order to improve the level of a reception signal and clearly distinguish between interference signals from other mobile stations and the original reception signal (Pg. 2, Lines 1-5).

As to claim 34, Sato discloses providing the sign inverted signal to phase offsetter circuitry by using at least one switch (Fig. 2, means 301).

As to claim 35, the instant application's disclosed prior art further teaches an amplitude adjustment circuit that adjusts the amplitude of the phase offset calculation intermediate components before being inputted to the phase-offsetter (e.g. SRI and SRQ; Fig. 4B, means 406 and 407). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the amplitude before the phase offset calculation step as taught by the instant application's disclosed prior art in order to improve the level of a reception signal (Pg. 2, Lines 1-5) and compensates for the amplitude variations of the signal to be received by the receiver.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is 571-272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Freshteh Aghdam
Examiner
Art Unit 2611

December 21, 2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER